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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,572	03/10/2000	Pascal Moniot	859063.463	5868

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EXAMINER	
SWICKHAMER, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
2662	//

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/523,572	MONIOT, PASCAL	
	Examiner	Art Unit	
	Christopher M Swickhamer	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-22* is/are allowed.

6)☒ Claim(s) *1-4,7,9-12 and 14, 15 and 17* is/are rejected.

7)☒ Claim(s) *5-6, 8, 13 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to the Amendment filed 12/22/03. Claim 16 has been cancelled. Claims 21 and 22 have been added. The amendments to claims 1, 7 and 12 have been entered. Claims 1-15 and 17-22 are pending. Claims 5, 6, 8, 13 and 18 are objected to for depending from rejected claims. Claims 1-4, 7, 9-12, 14, 15 and 17 are not in condition for allowance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7, 9-12 and 14, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Wicklund (USP 6,034,958).

- Referring to claim 1, Wicklund discloses a device for associating hash codes for table pointers (indexes) to ATM PHY/VPI/VCI addresses chosen from among a greater number of values than the number of available hash codes associated with table pointers (indexes, col. 2, lns. 45-col. 3, lns. 15), including: a search table (memory) containing table address locations associated with hash codes for table pointers (indexes) and respective PHY/VPI/VCI combination fields (check words) corresponding to bits having predetermined positions in the

ATM PHY/VPI/VCI addresses associated with the pointers (indexes, Fig. 4, col. 6, lns. 35-65, the PHY/VPI/VCI of the ATM address have a standardized format in the ATM cell and are placed in a predetermined position); a hashing (packing) circuit receiving a current ATM PHY/VPI/VCI address and suppressing in this address bits having said predetermined positions (Fig. 4, col. 5, lns. 45-67, suppress bits using a predetermined hash code which will inherently affect predetermined positions in the PHY/VPI/VCI address), the hash coded (packed) address provided by the hashing (packing) circuit being used to select in a read mode a search table (memory) location (Fig. 4, col. 5, lns. 57-67); and a comparator configured to indicate that the current ATM PHY/VPI/VCI address corresponds to the selected search table (memory) location when the bits of the PHY/VPI/VCI combination field (check word) of the selected search table location are equal to the corresponding bits of the current ATM PHY/VPI/VCI address (Fig. 4, col. 7, lns. 3-27).

- Referring to claim 2, Wicklund discloses the device of claim 1, wherein the device includes a VCI mask circuit that, according a predetermined VCI mask, annuls bits other than those suppressed by the hashing (packing) circuit, which also correspond to PHY/VPI/VCI combination (check word) bits (col. 4, lns. 50-col. 5, lns. 40).

- Referring to claim 3, Wicklund discloses the device of claim 1, wherein each search table (memory) location contains a High and Low pointer bits indicating whether the location is occupied by the PHY/VPI/VCI combination field indicates an illegal cell (col. 7, lns. 2-27).

- Referring to claim 4, Wicklund discloses the device of claim 1, wherein the addresses are ATM network addresses, and the indexes identify connections of the device to one or several ATM networks (col. 2, lns. 45-col. 3, lns. 15).

- Referring to claim 7, Wicklund discloses an address association device, comprising: a VCI masking circuit configured to receive a plurality of ATM address bits and mask the VCI address bits in accordance with a predetermined VCI mask pattern (col. 4, lns. 50-col. 5, lns. 40); a hashing (packing) circuit configured to receive ATM PHY/VPI/VCI address bits from the masking circuit and to reduce the number of ATM PHY/VPI/VCI address bits to a plurality of hash code (index) bits and to suppress from the address bits a plurality of PHY/VPI/VCI combination (check word) bits having predetermined positions in the ATM address bits according to a predetermined generating polynomial hashing (packing) pattern (col. 5, lns. 40-67, the PHY/VPI/VCI bits are at predetermined locations within the ATM address and are suppressed using a predetermined hashing code that inherently affects bits at predetermined locations); a search table (memory) configured to receive the plurality of pointer bits found from the hash code bits (index bits) and the plurality of PHY/VPI/VCI combination (check word) bits and to associate the received pointer (index) bits and PHY/VPI/VCI combination (check word) bits with the search table (memory) location of a network connection identified by the channel identifier (Fig. 4, col. 5, lns. 57-col. 6, lns. 12, col. 6, lns. 35-col. 7, lns. 3); and a comparator coupled to the search table (memory) and configured to receive the plurality of ATM PHY/VPI/VCI address bits and to indicate when selected bits from the plurality of ATM PHY/VPI address bits correspond to the plurality of PHY/VPI/VCI combination field (check word) bits associated with the search table (memory) location addressed in the plurality of address bits (col. 7, lns. 3-27).

- Referring to claim 9, Wicklund discloses the device of claim 7 wherein each network connection in the search table (memory) includes a High and Low pointer (enable) bits that are

configured to signal when the network connection in memory is an non-errored active connection to the network (Fig. 4, col. 7, lns. 2-27).

- Referring to claim 10, Wicklund discloses the device of claim 9, further comprising a search logic circuit coupled to the High and Low pointer (enable) bits and to the comparator and configured to indicate when a selected search table location addressed by the plurality of address bits is a non-errored active location (Fig. 4, col. 7, lns. 2-27).

- Referring to claim 11, Wicklund discloses the circuit of claim 7, further comprising a Pointer lookup table (register) configured to store a root (base) address corresponding to a beginning address in the search table (memory) and, further comprising an adder for adding the pointer containing the root (base) address to the hash coded address bits received from the hashing (packing) circuit (Fig. 4, col. 5, lns. 57-67).

- Referring to claim 12, Wicklund discloses a method for associating ATM PHY/VPI/VCI addresses to search table (memory) locations, comprising: receiving a plurality of ATM PHY/VPI/VCI address bits and VCI masking the address bits in accordance with a predetermined VCI mask pattern (Fig. 4, col. 4, lns. 50- col. 5, lns. 40); hashing (packing) the masked plurality of address bits to reduce the number of address bits to a plurality of hash coded (packed) address bits according to a predetermined generating polynomial (packing) pattern and suppressing PHY/VPI/VCI combination (check word) bits from the VCI masked address bits (col. 5, lns. 40-67), the check word bits having predetermined positions in the plurality of address bits (the PHY/VPI/VCI bits inherently have predetermined positions within the ATM address, the PHY/VPI/VCI are in separate fields within the ATM header); associating the hash coded (packed) bits with a pointer to a search table (memory) location corresponding to a

network connection identified by the channel identifier (Fig. 4, col. 5, lns. 57-67, col. 7, lns. 2-27); and comparing selected bits from the plurality of ATM PHY/VPI/VCI address bits for a selected search table (memory) location with selected PHY/VPI/VCI combination field bits associated with a search table (memory) location addressed in the plurality of address bits and indicating when there is a match (Fig. 4, col. 7, lns. 2-27).

- Referring to claim 14, Wicklund discloses the method of claim 12, further comprising logically combining (ANDing) an enable bit with the results of the comparing to determine if a selected memory location is a non-errored active connection.

- Referring to claim 15, Wicklund discloses the method of claim 12 wherein hashing (packing) comprises storing a base pointer lookup table address corresponding to a pointer to a root (beginning) address in a search table (memory) and the method further comprises adding the base pointer lookup table address to the hash coded (packed) address bits reduced during hashing (packing) to determine the root search table address (Fig. 4, col. 5, lns. 40-67, col. 6, lns. 65-col. 7, lns. 27).

- Referring to claim 17, Wicklund discloses the method of claim 14, further comprising disabling an enable bit corresponding to a memory location selected by the plurality of address bits when the memory location is occupied. The search table inherently contains a bit indicating whether the location is occupied or not that can be disabled or enabled based on the occupation status of the location. The system must have some way of identifying which locations contain the PHY/VPI/VCI combination fields.

Allowable Subject Matter

4. Claims 5, 6, 8, 13 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- Claims 19 and 20 are allowable for reasons indicated in the previous Office Action, paper No. 7.

- Claims 21 and 22 are allowable for containing subject matter objected to in claim 8. Claims 21 and 22 are similar to the combination of claims 1 and 8 and are allowable for the same reason claim 8 is objected to.

Response to Arguments

5. Applicant's arguments filed 12/22/03 have been fully considered but they are not persuasive.

- Referring to the argument on page 9, lines 12-15, Applicant argues that Wicklund does not teach or suggest suppressing the address bits having "predetermined positions" as described in claim 1, Applicant states that the polynomial has variables that do not correlate in any way to predetermined bits. The applicant also argues that the hash coding of Wicklund is a fundamental feature to the invention that teaches away from the claimed invention. The Examiner respectfully disagrees. Claim 1 states that the check words correspond to bits having predetermined positions in the addresses (lns. 3-4). Claim 1 further states that the packing circuit suppresses in this address bits having said predetermined positions (lns. 6-8). Wicklund teaches

compressing the PHY/VPI/VCI combination (check word) from the ATM address using a hashing function (Fig. 4, col. 2, lns. 49-60, col. 8, lns. 47-53). The PHY/VPI/VCI have predetermined position in the standard ATM cell used by Wicklund. The hash function suppresses bits from the PHY/VPI/VCI using a hash code to compress the PHY/VPI/VCI information (col. 2, lns. 49-65, col. 5, lns. 40-57). The hash code compresses the data by appending 14 zeros to the 33 bit PHY/VPI/VCI address, and dividing the polynomial of degree 47 by a polynomial of degree 14. This process acts on the PHY/VPI/VCI address in a predetermined way, by affecting predetermined bits based on the hash code. By selecting the hash code, this determines the predetermined bits of the PHY/VPI/VCI address that will be suppressed. Since the claim has not defined how the bits are predefined within the address or how the packing circuits suppresses data within the address differently from hashing function, the Examiner believes that the claim is not patentably distinct from the Wicklund reference. For this reason, the Examiner believes the rejection is proper.

- Referring to the argument on page 10, lns. 2-5, the applicant argues that Wicklund does not teach or suggest having check words having predetermined positions in the address associated with indexes and packing the current address and suppressing the address bits having predetermined positions. The Examiner respectfully disagrees. Wicklund teaches using PHY/VPI/VCI information (check words) having predetermined positions in the ATM address which are associated with hash codes used to select pointers (indexes) to the search table (Fig. 4, col. 5, lns. 58-67), the system hashes the current address (incoming information on PHY/VPI/VCI from an incoming ATM cell) and suppresses the address bits having predetermined positions (col. 2, lns. 49-65). The hash code uses a polynomial based on the

PHY/VPI/VCI information to suppress in the data from the ATM address using the hash code which will affect predetermined positions within the PHY/VPI/VCI information based on the hash code selected (col. 5, lns. 40-57). The system of Wicklund and the claimed invention have similar features. Since the claim has not defined how the predetermined bits are suppressed using the packing function, or how the bit positions in the check word correspond to the predetermined positions, the Examiner believes that rejection is proper.

- Therefore, the Examiner believes that the rejections under 102(e) to the claims are proper.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M Swickhamer whose telephone number is (703) 306.4820. The examiner can normally be reached on 8:00-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CMS
March 17, 2004

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